REMARKS

Specification

The disclosure has been objected to because of informalities. Applicant has amended the specification to correct these informalities.

Claim Rejections - 35 U.S.C. § 112

The Examiner has rejected claims 6 and 12 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant has amended claims 6 and 12 to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. As such, Applicant respectfully requests the removal for the 35 U.S.C § 112, second paragraph rejection of claims 6 and 12.

Double Patenting

Claim 12 has been objected to under 37 C.F.R. § 1.75 as being substantial duplicate of claim 6. Applicant has amended claim 7 upon which claims 12 depends and accordingly, claim 12 is patentably distinct from claim 6. As such, Applicant respectfully requests the removal of the objection of 37 C.F.R. § 175.

Claim Rejections – 35 U.S.C. § 102/103

The Examiner has rejected claims 1-2, 4-8 and 10-12 under 35 U.S.C. § 102(b) as being anticipated by Maegawa ('513). The Examiner has rejected claims 2 and 9 under 35 U.S.C. § 103(a) as being unpatentable over Maegawa ('513) in view of Yu ('869).

In claims 1-12, applicant teaches and claims a nonplanar transistor having a gate electrode which fully wraps around the channel region or almost wraps all the way around the channel region.

In one embodiment of the present invention, a two step etch process, which includes an anisotropic etch (Figure 6E) followed by an isotropic etch (Figure 6F), is used to form the gate electrode. The anisotropic etch defines the gate electrode and the isotropic etch removes gate electrode material from regions underneath the semiconductor body so that undesired "stringers" are not left which can short the source and drain regions to the gate electrode. The two step etch process illustrated in Figures 6E and 6F forms a gate electrode where the bottom portion undercuts the top portion as illustrated in Figure 6G and claimed by applicant in claims 1-6.

It is Applicants understanding that Maegawa fails to disclose a gate electrode where the bottom portion laterally undercuts the top portion as claimed by Applicant in claims 1-6. Applicant understands Maegawa to disclose, in each of his embodiments, a gate electrode where the bottom portion and the top portion have the same dimensions. Accordingly, Maegawa fails to teach Applicant's invention in claimed in claims 1-6. Applicant, therefore, respectfully respects the removal of the 35 U.S.C. §§ 102 and 103 rejections of claims 1-6 and seeks an early allowance of these claims.

Additionally, in another embodiment of the present invention, the gate electrode is formed with a replacement gate process. In such a process a dielectric film is formed over and around the semiconductor body and an opening is formed in the dielectric film to expose the semiconductor body. The use of an isotropic etch results in a larger opening 705 formed in the insulating substrate than the opening 704 formed in the dielectric film. (Figure 7A and Figure 8E) A portion of the insulating substrate is then removed using an isotropic etch to under cut and expose at least a portion of the bottom surface of the semiconductor body. (Figure 7B and Figure 8F) After forming a gate dielectric layer on the top surface and sidewalls of the semiconductor body as well as on the exposed portion of the bottom surface, a gate electrode material is blanket deposited over the dielectric film and into the opening. The gate electrode material is then removed from the top surface of the dielectric film to define the gate electrode. (Figure 7C/7D and 8G) The resulting gate electrode has a top portion above the insulating substrate and a bottom portion formed in the insulating substrate wherein the bottom portion is wider than the top portion as claimed in claims 7-12.

It is Applicants understanding that Maegawa fails to disclose a gate electrode which has a top portion above an insulating substrate and a bottom portion formed in the insulating substrate wherein the bottom portion is wider than the top portion as claimed in claims 7-12. It is Applicants understanding that Maegawa discloses in every one of his embodiments a gate electrode where the bottom portion and the top portion have the same dimensions. Accordingly, Maegawa fails to teach or render obvious Applicant's inventions as claimed in claims 7-12. Applicant, therefore, respectfully respects the removal of the 35 U.S.C. §§ 102 and 103 rejections of claims 7-12 and seeks an early allowance of these claims.

Pursuant to 37 C.F.R. § 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. §§ 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,
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